REMARKS

Initially, Applicants thank the Examiner for the courtesies extended to their representatives during telephone interviews conducted during the week of May 19, 2003. While Applicants appreciate the suggestions kindly made by the Examiner during those interviews, Applicants believe that the claims, as amended, define over the art. In view of these amendments, favorable reconsideration and further examination are respectfully requested.

Claims 1 to 23 are pending in this application, of which claims 1 and 18 are the independent claims. Claims 1 to 3, 5 to 9, 12, 13, and 17 to 19 were rejected under 35 § U.S.C. 102(b) as being anticipated by Panchou et al.

Claim 1, as amended, is directed to a semiconductor structure that includes a semiconductor substrate and a compliant interconnect element disposed on a first surface of the substrate. The compliant interconnect element includes a portion raised from the first surface of the substrate that defines a chamber between the first surface of the substrate and the portion of the compliant interconnect element.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, Panchou is not understood to disclose or to suggest a compliant interconnect element that includes a portion raised from the first surface of the substrate defining a chamber between the first surface of the substrate and the portion of the compliant interconnect element. In this regard, Panchou discloses a compliant element 30 that is flat. No portion of the compliant element 30 shown in Panchou is raised above a surface of the substrate to form a chamber.

Furthermore, the alleged "vias" shown in Panchou are merely holes that extend completely through the compliant element. None of these so-called vias are formed in conjunction with a portion of the compliant element that is raised from the substrate.

Thus, as understood by Applicants, Panchou does not disclose or suggest at least a portion of a compliant interconnect element raised from a first surface of the substrate that defines a chamber between the first surface of the substrate and the portion of the compliant interconnect element. For at least this reason, claim 1 is believed to be in condition for allowance.

Claim 18 roughly corresponds to claim 1 and, therefore, is believed to be allowable for at least the same reasons as claim 1 noted above.

Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the above address. Applicants' attorney can be reached by telephone at the number shown above.